Fault Current Interruption by the Simplified Dynamic Voltage Restorer to Enhancing Power Quality

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Abstract - **This paper presents a control scheme for the purpose of interrupting the fault current by the DVR (Dynamic Voltage Restorer) which is present on down-stream side of the DVR. The control scheme provides compensation for the voltage sags. PLL is not required in this scheme and it can control the magnitude and phase angle of the injected voltage independently. To estimate the magnitude and phase of the measured voltages, FLES digital filters are used. These are capable of to reduce the impacts of noise and harmonics. The simulation is performed in the MATLAB/simulink software. The proposed scheme i) can interrupt the fault current within two cycles ii) limits the dc link voltage rise so that no restrictions iii)gives satisfactory operation under arcing fault conditions also iv) can interrupt the fault current under low dc link voltage conditions. Using series active filter power quality can be enhanced.**

I. INTRODUCTION

DVR is used to counteract voltage sags by injecting controlled three-phase ac voltages in series with the supply voltage and to enhance the quality of voltage by adjusting voltage magnitude, wave shape and phase angle. In general, DVR is bypassed during down-stream fault in order to protect the components of the DVR against the high fault currents.

A control scheme for DVR to function as fault current limiter is provided in. The main drawback of this scheme is that the dc link voltage rise due to real power absorption. The dc link voltage rise can be mitigated at the cost of a slow decaying dc fault current component using the methods proposed.

To overcome the limitations which are mentioned above, this paper introduces a control strategy for DVR such that voltage sag compensation under balanced and unbalanced conditions and a function of interrupting the fault current. The former function has been presented in and the latter is in this paper. Limiting fault current by the DVR disables the main and backup protection (e.g. over current relay). This can result in prolonging the duration fault. Thus, it is preferred to reduce the fault current to zero and send a trip signal to the upstream relay. FCI function requires 100% voltage injection capability. Thus, power ratings of the series transformer and the VSC would be three times the conventional DVR. This would result in more expensive DVR system. Economic feasibility of such a DVR depends on the importance of the load protected by the DVR and the cost of DVR itself. The performance of the proposed control strategy is evaluated through simulation in MATLAB/Simulink.

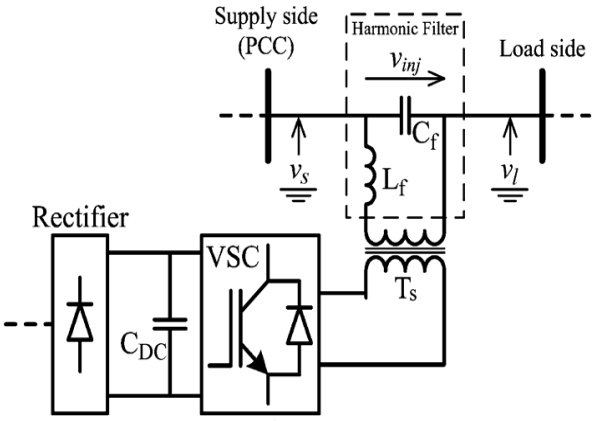

Fig.1. Schematic diagram of a DVR with a line-side harmonic filter.

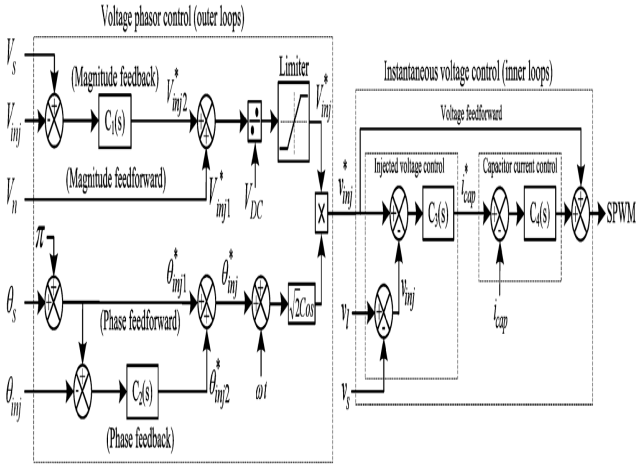

Fig. 2 Per-phase block diagram of the DVR control system In FCI mode.

II. PROPOSED FCI CONTROL STRATEGY

The adopted DVR converter is comprised of three independent H-bridge VSCs that are connected to a common dc-link capacitor. These VSCs are series connected to the supply grid, each through a single-phase transformer. The proposed FCI control system consists of three independent and identical controllers one for each single-phase VSC of the DVR.

A. Voltage phasor control system

In the FCI operation mode, the required injected voltage phasor is equal to the source voltage phasor but in phase opposition. The performance in terms of transient response, speed and steady-state error is enhanced by independent control of the magnitude and phase. The steady-state errors of magnitude and phase of the injected voltage can be eliminated by using two PI controllers (C_1 and C_2). Parameters of each controller are determined to achieve a fast response with zero steady-state error. The output of voltage phasor control system is a reference phasor V^*_{inj}.The magnitude and phase angle of V^*_{inj} are independently calculated and passed through a limiter. The resulting magnitude and phase angle are converted to the sinusoidal signal V^*_{inj} and is given as a reference signal to the instantaneous voltage control.

B. Instantaneous voltage control system

Under ideal conditions, voltage sag compensation is done if the output of the output of the phasor based controller V^*_{inj} is directly fed to the SPWM unit. However, resonances of harmonic filter can't be eliminated. Therefore, to improve dynamic response and stability of the DVR, an instantaneous injected voltage controller and a harmonic filter capacitor current controller are used to attenuate resonances. The generated reference signal V^*_{inj} is compared with the measured injected voltage V_{inj} and the error is fed to the voltage controller.

The output of the voltage controller i^*_{cap} acts as a reference signal for the filter capacitor current control loop. This i^*_{cap} is compared with the measured capacitor current i_{cap}, and error is fed to the current controller. The Steady state error of the system is fully eliminated by the PI controller in the outer control loop. Therefore, there is no need for higher order controllers in the inner control loop. If a large value of k_V is used, it results in amplification of the DVR filter resonance and has adverse impact on the system stability.

Thus, the transient response of the DVR is enhanced by feed forward loop and a small proportional gain is utilized as the voltage controller. A large k_C damps the harmonic resonance but it is limited by practical considerations. Therefore the lowest value of the proportional gain which can effectively damp the resonances is used. The output of the current controller is added to the feed forward voltage to derive the signal for the PWM generator.

In FCI mode, the injected voltage phasor should be equal to the source voltage phasor but in opposite direction. The voltage phasor control block consists of two PI controllers (C_1 and C_2) that are used to eliminate steady state errors of the magnitude and phase of the injected voltage. The output phasor of this block is $V^*_{(inj)}$. To make the injected voltages free from the effect of dc-link voltage variations, $V^*_{(inj)}$ normalized by V_{dc}. Ideally voltage sag can be compensated effectively if the output of voltage phasor control is directly fed to the sinusoidal pulse width modulation(SPWM) unit. However, resonances of harmonic filter can't be eliminated. Therefore to improve transient stability and dynamic response of DVR, an instantaneous injected voltage controller and a harmonic filter capacitor current controller are used to attenuate resonances. The generated reference signal for $V^*_{(inj)}$ is compared with the measured injected voltage $V_{(inj)}$ voltage controller.

III. STUDY RESULTS

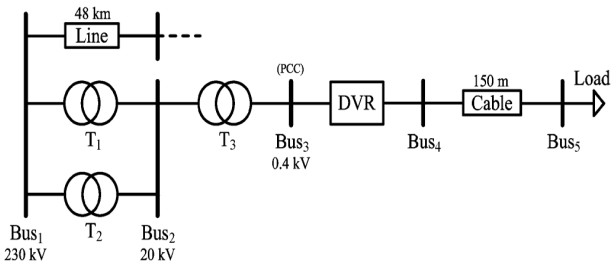

Fig.3.Single-line diagram of the system used for simulation studies.

Fig. 3 depicts a single-line diagram of a power system This is used to evaluate the performance of the proposed DVR control system under different fault scenarios, in the PSCAD/EMTDC software environment. A 525-kVA DVR system is installed on the 0.4-kV feeder, to protect a 500-kVA, 0.90 lagging power factor load against voltage sags.

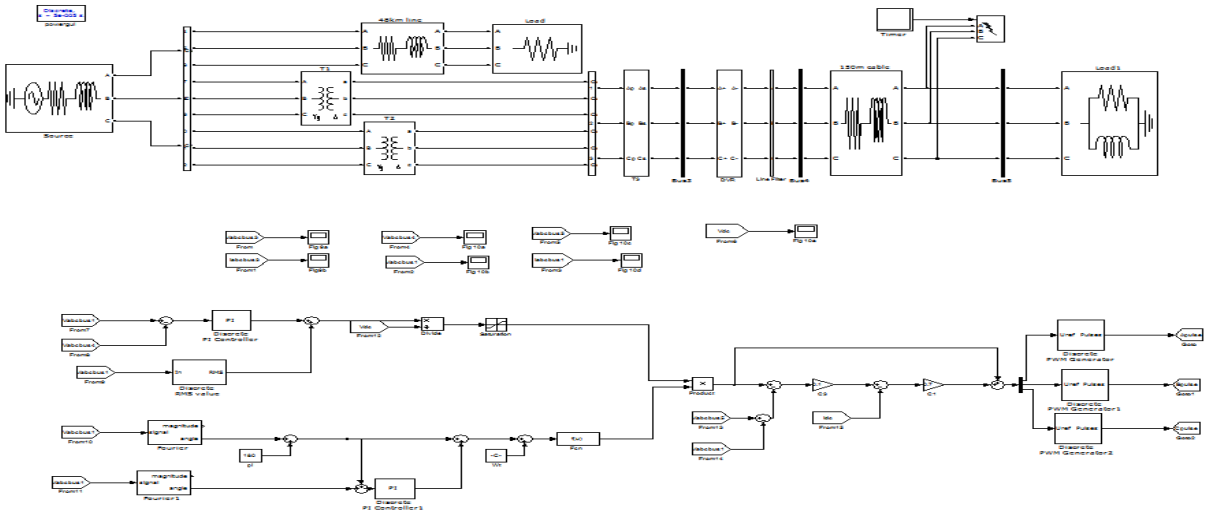

Fig.4.Simulation block diagram of three phase downstream fault Interruption with DVR

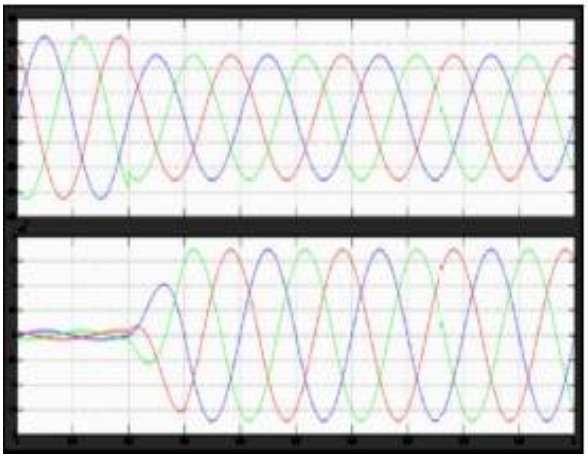

Fig. 5 a) Voltages at bus3 b) fault currents, during 3phase fault when DVR is bypassed.

A. Three-Phase Downstream Fault

The system is subjected to a three-phase short circuit with an eligible fault resistance at t = 20 ms at Bus5. Prior to the fault inception, the DVR is inactive (in standby mode) (i.e., the primary windings of the series transformers are shorted by the DVR). During the fault if the DVR is bypassed, the voltage at Bus3 drops to 0.77 p.u. and the fault current increases to about 17 times the rated load current.

B. Phase-to-Phase Downstream Faults

The system is subjected to a phase-A to phase-C fault with the resistance of 0.05Ω at 10% of the cable length connecting Bus4to Bus5, at t = 20 ms. When the DVR is inactive (bypassed) during the fault , the PCC voltage drops to 0.88 p.u., and the fault current increases to about 11times the rated load current.

C. Single-Phase-to-Ground Downstream Fault

Phase-A of the system is subjected to a fault with the resistance of 0.2Ω at 10% length of the cable connecting Bus4to Bus5, at t = 20 ms. If the DVR is inactive, the PCC voltage does not considerably drop and the fault current is about 2.5 p.u. It must be noted that although the PCC voltage drop is not considerable, the fault current must be interrupted by the DVR to prevent possible damages to the VSC before the fault is interrupted by the relays. The reason is that the operation time of the over current relays is considerable for a fault current of about 2.5p.u

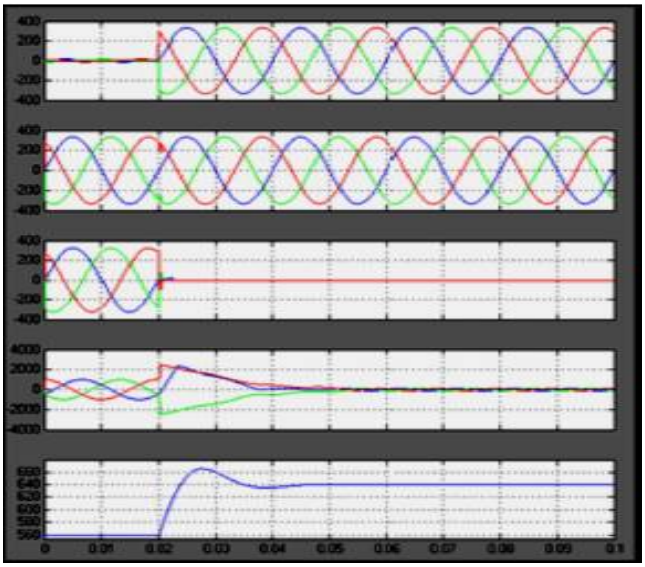

Fig. 6 (a) Injected voltages. (b) Source voltages. (c)Load voltages. (d) Line currents. (e) DC during the three-phase downstream fault.

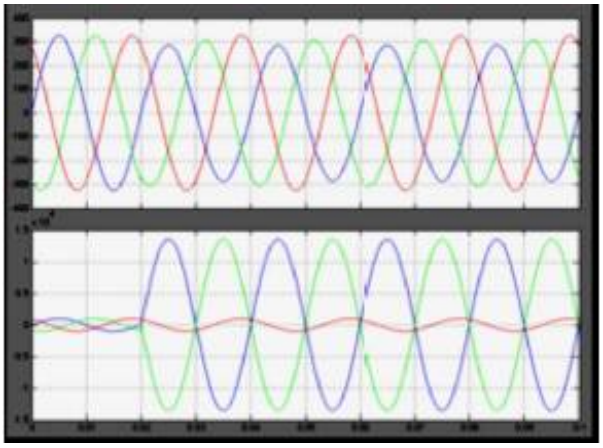

Fig. 7(a) Voltages at bus, (b) Fault currents, during Downstream phase-to phase fault when the DVR is Inactive (bypassed).

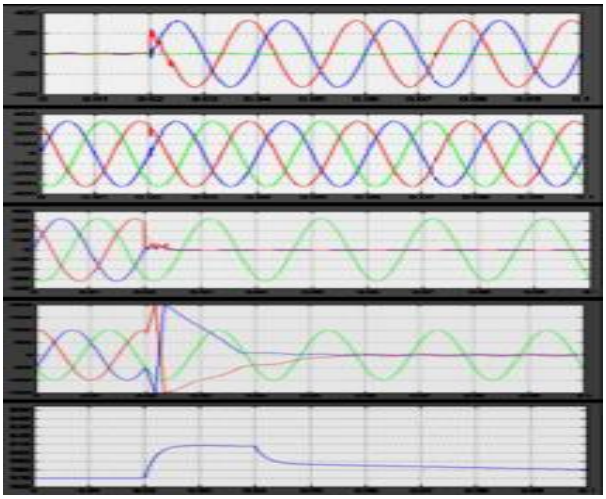

Fig. 8 (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC during the Phase-to-phase downstream fault.

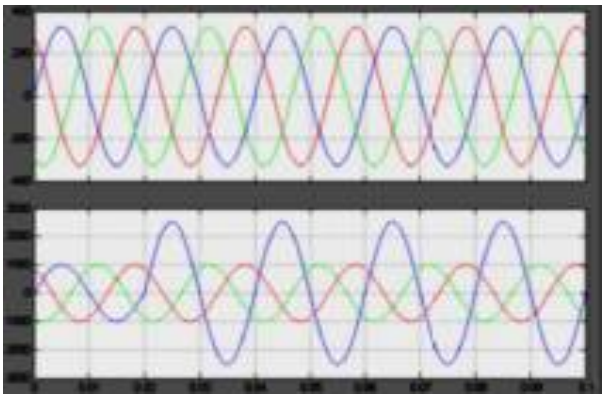

Fig. 9 (a) Voltages at bus 3(b) Fault currents, during the downstream single phase-to-ground the DVR is Inactive (bypassed).

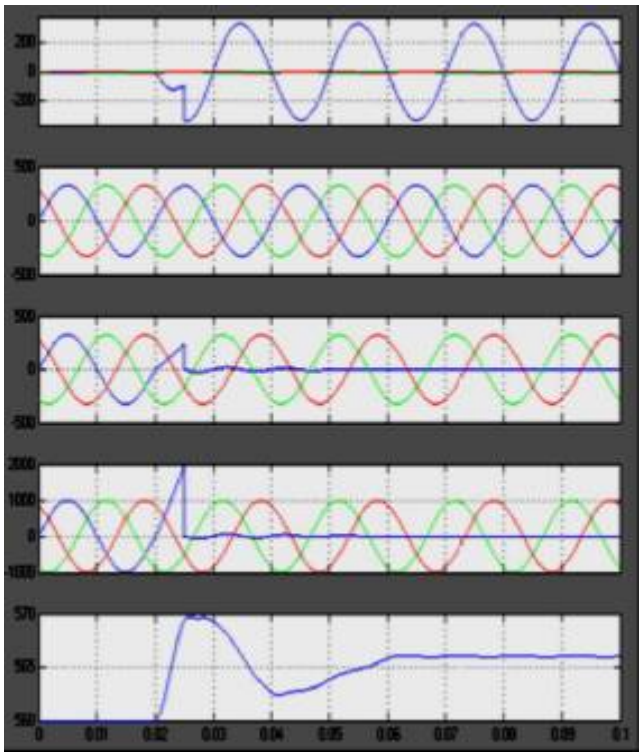

Fig. 10 (a) Injected voltages. (b) Source voltages. (c)Load voltages. (d) Line currents. (e) DC During the phase-to-ground downstream fault.

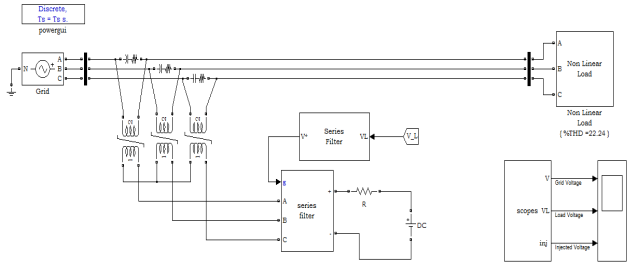

Fig. 11 Series active filter for power quality enhancing.

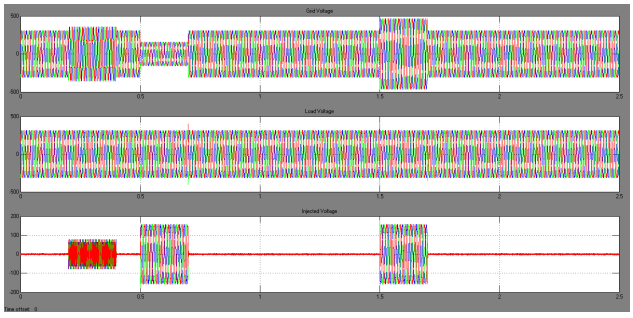

Fig. 12 grid, load, injected voltage waveforms.

IV. CONCLUSION

The proposed multi loop control system provides a desirable transient response and steady-state

performance and effectively damps the potential resonant oscillations caused by the DVR LC harmonic filter. The proposed control system detects and effectively interrupts the various downstream fault currents within two cycles (of 50 Hz). In future enhancement simultaneous operation of Fault current interruption and voltage sag compensation can be obtained by Dynamic voltage restorer. And by using series active filter it is clearly shown that the power quality can be improved.

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